Q & A with Louie De Luna, Director of Marketing, ALDEC

Q: Louie, tell me a little about ALDEC. What is the primary function/product output and what is the target demographic in the financial vertical?

A: ALDEC was established in 1984. We are a verification technology and tool provider for FPGAs and ASICs. We are one of the pioneers in mixed-language RTL simulation and hardware-assisted verification, and we continue to support our customers in the areas of telecommunication, high performance computing and embedded systems. Using our FPGA verification tools, methodologies and expertise we would like to help the HFT industry to accelerate algorithms and data processing using FPGAs.

Q: Measuring the value of FPGA enhanced functionality is a big focus for determining if, when and how a firm should be using FPGA and acceleration technologies. Can ALDEC help with this?

A: The inherent re-programmability of FPGAs, deep pipelining structures and massive parallel compute resources have made FPGAs popular in HFT. The re-programmability aspect allows for new protocols to be supported using the same FPGA hardware. The reconfigurable parallelism of FPGA and availability of high speed serial IO with controllers supporting fiber links allow for a predictable and ultra-low latency.

It is important to say FPGA is not an acceleration cure for every algorithm and data processing. FPGA are best to use for acceleration of algorithms where huge number of operations is performed on relatively small data. Expertise in FPGA definitely helps to achieve the best possible results considering the architecture and features. As a company, we have huge expertise in RTL porting and optimizations which can help CTO's and Engineers in the financial vertical.

Q: Talk to me a little about the RTL Simulator for support. This sounds like a unique tool that can go a long way in having firms exploring their best use case(s) for FPGA.

A: We've had our mixed-language RTL simulation technology for around 30 years now and we continue to enhance it. Our tool supports various language standards such as Verilog, VHDL, SystemVerilog(UVM) and SystemC for both Windows and Linux OS. Simulation is a standard part of the FPGA development flow employed prior to running the design in the FPGA board. Simulation enables engineers to check and debug the design for various test scenarios and strategies, where they have full visibility into the FPGA pin I/Os, internal registers and signals. Engineers can debug the design without having to re-compile the FPGA binaries, and optimize the design for performance before running it in the FPGA board.

We have many users in the HFT market using our Riviera-PRO High Performance RTL Simulator with Python and Cocotb for creating complex verification testbenches with minimal effort. Cocotb is open-source co-routine based co-simulation library for writing HDL testbenches in Python. I've seen an RTL implementation of an IP block for packet parsing where the verification effort took 30 days with 5,000

lines of UVM testbench code, but this only took 1 day with 500 lines of Python/Cocotb testbench code. Interestingly, this particular UVM testbench code failed to see some bugs that were found using Python/Cocotb. Simulation is crucial to saving time and adding to the success of your FPGA usability.

The combination of advanced debugging features in Riviera-PRO is also a big productivity booster. The debugging features that are commonly used in HFT are Code Coverage, Xtrace, Waveform Viewer, Advanced Dataflow and Post-Simulation Debug.

Q: An issue that firms grapple with is the budget balancing and examining the equation of speed vs. capacity. How would ALDEC approach this?

A: The base of HFT solutions is the FPGA board with the addition of external resources like memories. Different algorithms may need different resources, for example some may need more DSP primitives and require that type of FPGA, and some may need multiple small memories for transactions with parallel tasks executed in FPGA. It is important that the FPGA board provider is able to deliver different configurations with ability to start from basic one and scale it to multiple instances. Aldec offers whole family of boards based on Xilinx Virtex-7 and UltraScale in multiple configurations and software to manage them.

Q: What are some key differentiators that ALDEC can provide to the latency sensitive trading community?

A: In addition to the verification tools and FPGA boards that we provide, we also offer RTL porting services. The ability to provide services that cover development, testing and execution in FPGA is key to success. A good example that we provide is PCIe based infrastructure for maximum throughput with the industry standard AMBA AXI interface to connect user module/algorithm in FPGA, which enables high bandwidth host to FPGA channel to be integrated with low latency cores. The simulation we provide ultimately saves latency focused traders time, efficiency and money.